IN THE SPECIFICATION:

Please amend the paragraph at page 1, lines 15-19, as follows:

-- Fig. 1 shows a conventional internal voltage generator 1, a conventional address circuit 2 and a conventional data output circuit 3. The internal voltage generator 1, the address circuit 2 and the data output circuit 3 are separated as an individual circuit in the conventional memory devices.--.

Please amend the paragraph at page 2, line 23 to page 3, line 9, as follows:

-- There is provided an internal voltage generator of a semiconductor device comprising a tuning unit, a characteristic controller and an internal voltage ~~generator~~ generating unit. The tuning unit receives a test mode signal, an external signal and a signal stored in an internal setup device, and outputs a control signal. The characteristic controller receives the control signal, and outputs a characteristic controlling signal. The internal voltage ~~generator~~ generating unit receives a reference input signal and the characteristic controlling signal, and controls a characteristic of an internal voltage.--.

Please amend the paragraph at page 3, lines 12-14, as follows:

-- Fig. 1 shows a conventional internal voltage generator, a conventional address circuit and a conventional data output circuit, which are separated from each other.--.

Please amend the paragraph at page 4, lines 8-9, as follows:

-- Fig. 7 is a detailed circuit diagram illustrating a demultiplexer in a first test mode block of ~~Fig. 1~~ Fig. 2.--.

Please amend the paragraph at page 6, lines 5-7, as follows:

-- The ~~test voltage output unit~~ data output circuit 300 comprises a multiplexer 310 for outputting a signal, which is from the VCore driver 50 or the Dout buffer 70, into a DQ pad 71.--.

Please amend the paragraph at page 6, line 24, to page 7, line 13, as follows:

-- A common source of the PMOS transistors P1 and P2 is connected to a power VCC, and a common gate of the PMOS transistors P1 and P2 is connected to a drain of the PMOS transistor P2. A drain of the PMOS transistor P1 is connected to a drain of the NMOS transistor

N1, and the drain of the PMOS transistor [[~~P1~~]] P2 is connected to a drain of the NMOS transistor N2. A common source of the NMOS transistors N1 and N2 is connected to a drain of the NMOS transistor N3. A gate of the NMOS transistor N1 receives an input signal 'input'. An output unit B of the second amplifier is fed back to a gate of the NMOS transistor N2. A gate of the NMOS transistor N3 receives an input signal 'bias'. An output node of the first amplifier is the drain (A) of the PMOS transistor P1.--.

Please amend the paragraph at page 7, line 19, to page 8, line13, as follows:

-- The two-step amplifier is a system having two [[~~pole~~]] poles. Here, a phase margin of more than 60° should be secured for frequency stability. The phase margin refers to a difference between phase response and -180° when an amplitude response is 0dB. In order to secure the phase margin of the system, a "Miller compensation method" is used to improve stability. Here, a capacitor is connected between input and output terminals of the second amplifier to separate two main poles. In the "Miller compensation method", a feed-forward path from a terminal A to a terminal B is formed. The feed-forward path causes a zero to be generated on a right half ~~plane.~~ plane. A RC selection unit 410 where capacitors and resistors are connected in series is used to remove the zero point. Additionally, an R selection unit 420 connected between the terminal (B) and an output terminal in cooperation with a capacitor C1 connected between the output terminal and ground generates a zero at a position of a second pole. As a result, the phase margin is improved by compensation effect.--.